Measurement of important circuit parasitics for switching transient analysis of SiC MOSFET and Schottky diode pair

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***Abstract*—Characterization of external circuit parasitics are important to study the switching dynamics and adverse effects related to that. This paper presents a set of simple experimental measurement techniques to determine different external circuit parasitics relevant for switching transient study of Silicon Carbide (SiC) MOSFET and Schottky barrier diode (SBD) pair. The simulation and experimental results confirm the accuracy of the presented method over a range of operating conditions for a 1.2-kV discrete SiC MOSFET and SBD pair.**

***Index Terms*—SiC MOSFET,SiC SBD, switching transient, parasitics measurement**

I. Introduction

Si has reached it's material limit. So to cater the need of high power density and high efficient power electronic converter, wide bandgap (WBG) devices are gaining popularity. SiC MOSFET belongs to the class of WBG power devices and in a close competition with Si IGBTs due to it's fast switching dynamics and lower on state resistance [1].

Fast switching transient reduces switching loss and helps to increases the switching frequency of power electronic converter. But it results in higher di/dt and dv/dt rate and excites circuit parasitics which depends both on device structure and package as well as circuit layout. This results into prolonged oscillations, over voltage stress and electromagnetic interference (EMI) noise during switching transient [2], [3]. Circuit parasitics can also affect the switching dynamics and incur additional switching loss [3], [4]. So to understand the switching dynamics and it's adverse effects, characterization of circuit parasitics are important. Nonlinear depletion capacitances are internal to the device and values are given in the datasheet as a function of voltage [5]. On the other hand, characterization of external circuit parasitics which comes from device package as well as circuit layout is required. This paper concerns with the characterization of external circuit parasitics of SiC MOSFET and Schottky diode pair.

Two different approaches are widely used in literature to characterize the circuit parasitics: 1. computation based approach and 2. measurement based approach. In computation based approach, software tools such as ANSYS MAXWELL 3D or StatMod can be used which uses finite element analysis (FEA) or partial element equivalent circuit (PEEC) method [6], [7]. Though accurate but this approach requires long computation time and suffers from convergence problem when physical structure is complex. It is also difficult and time consuming to derive an accurate geometrical model of a complex structure. Measurement based approach can be subdivided into two categories: time domain reflectometry (TDR) measurement and frequency domain impedance measurement. TDR measurement is based on transmission line theory [8]. Though accurate it requires specially designed hardware, expensive measurement equipment and software. Also TDR measurement method is generally developed for 50Ω connector impedance and suffers from lack of accuracy when the characteristic impedance of the device under test (DUT) deviates significantly from 50Ω. On the other hand, in frequency domain impedance measurement method impedance between two ports at different frequencies using a vector network analyser (VNA) [9]. As some of the internal device capacitances are nonlinear function of voltage, so it is difficult to find out external circuit parasitics from frequency domain impedance measurement.

In this paper, a simple and low cost measurement method of external circuit parasitics is presented. The external circuit parasitics are power loop inductance (L_d), common source inductance (L_s), external gate drain capacitance ($C_{g'd(ext)}$) and external anode cathode capacitance ($C_{ak(ext)}$) as it plays significant role in switching dynamics [3], [4].

II. Circuit for switching transient study

Equivalent circuit to capture the switching transient is shown in Fig. 1. Inductive load switching has been considered as it is common in most of the power electronic converters. SiC SBD is used in conjunction with SiC MOSFETs for most of the practical applications due to it's better performance indices [1]. SiC MOSFET is modelled as a three terminal device with terminals named as gate (g), drain (d) and source (s). Similarly SiC SBD has two terminals anode (a) and cathode (k).

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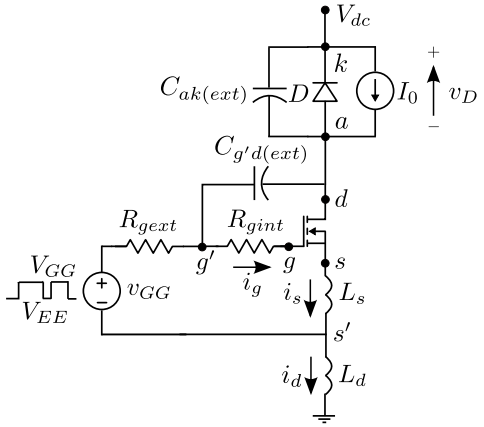

Fig. 1. Circuit configuration for switching transient analysis

v_{GG} is the applied gate driver voltage with two levels V_{GG} and V_{EE} respectively. R_{gext} and R_{gint} are the external and the internal gate resistance of the MOSFET. The effective gate resistance, R_g is the summation of R_{gext} and R_{gint}. External circuit parasitics that have been considered are following (Fig. 1):

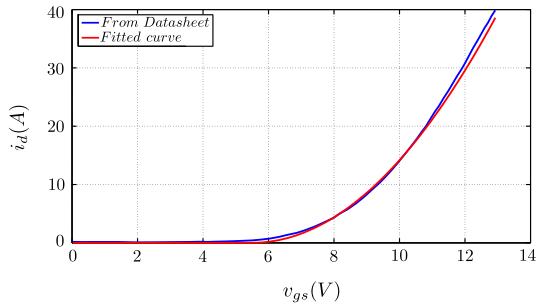

Fig. 2. i_d vs. v_{gs} curve for C2M0080120D from Wolfspeed, $V_{th} = 5.5V$, $\beta = 1.4A/V^2$

During switching transition, switching trajectory traverses through the saturation region for most of the time period. So to capture the switching dynamics through simulation, it is important to model the channel current (i_{ch}) accurately in the saturation region. Channel is in cut-off region for $v_{gs} < V_{th}$ and i_{ch} is equal to zero. Here V_{th} is the threshold voltage of the SiC MOSFET. For $v_{gs} > V_{th}$ and $v_{ds} > (v_{gs} - V_{th})$, MOSFET is in saturation region and the channel current i_{ch} can be modelled by (1) (taking long channel approximation). Transfer characteristics (in saturation region) of the MOSFET (i_d vs. v_{gs}) is given in the data-sheet for a given temperature. V_{th} and β can be obtained by fitting the transfer characteristics to the above equation (Fig. 2). V_{th} and β both are temperature dependent parameters.

$$i_{ch}(v_{gs}, v_{ds}) \approx \frac{\beta}{2}(v_{gs} - V_{th})^2 \tag{1}$$

- **Power loop inductance** (L_d): This is the summation of the DC bus inductance, the lead inductances of the MOSFET and the diode, and connection inductance between the MOSFET and the diode. L_d increases the voltage overshoot during turn off and results in power loop oscillation.
- **Common source inductance** (L_s): This is part of both gate and power loops. L_s reduces the di_d/dt rate and prolongs the current rise and fall time. This results in an increase in switching loss.
- **External gate to drain capacitance** ($C_{g'd(ext)}$): External parasitic capacitance across the g' and d terminal. $C_{g'd(ext)}$ prolongs the voltage fall and voltage rise time during turn on and turn off respectively and increases the switching loss on the active device.
- **External diode capacitance** ($C_{ak(ext)}$): External parasitic capacitance across the diode terminal ($C_{ak(ext)}$). $C_{ak(ext)}$ increases the channel current during the voltage fall of the active device and it also gets reflected on the switching loss of the active device.

The effect of external parasitic capacitance between d and s terminal of the MOSFET is neglected due to it's negligible value compared to the drain to source depletion capacitance of the SiC MOSFET. Due to the presence of the external circuit parasitics, it is not possible to measure $v_{gs}(t)$, $v_{ds}(t)$ and the channel current (i_{ch}) experimentally. So to obtain the actual switching loss accurately from simulation or using analytical loss estimation technique, determination of external circuit parasitics is important [4].

III. L_d AND L_s MEASUREMENT

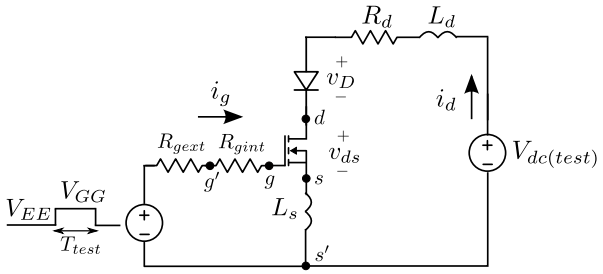

Fig. 3. Circuit configuration for parasitic inductance measurement

Circuit configuration of Fig. 3 is used to measure the parasitic inductances L_d and L_s. Same SiC SBD diode is used such that L_d value remains unaltered. It is connected in reverse way compared to Fig. 1. The test is carried out by giving a gate pulse of duration T_{test} and gate voltage V_{GG}. $V_{dc(test)}$ is chosen ($5V$, much smaller value compared to the rated voltage) such that the settling time of the gate circuit is much smaller compared to T_{test}. Maximum value of T_{test} is limited by the fact that the MOSFET should remain deep into ohmic region. T_{test} is in the range of few hundreds of nanosecond, so it can be assumed that the device temperature remains equal to ambient temperature.

For most of the test duration $v_{g's'} \approx V_{GG}$ (Fig. 4(a)), $i_g \approx 0$. Then $v_{gs'} \approx V_{GG}$ and $v_{gs} \approx (V_{GG} - L_s(di_d/dt))$. Practically $L_s(di_d/dt) \ll V_{GG}$, so $v_{gs} \approx V_{GG}$. In ohmic region,

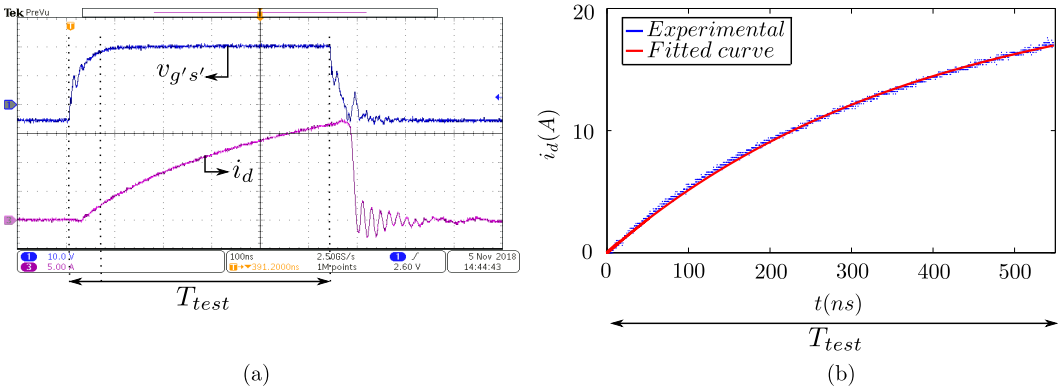

Fig. 4. Parasitic inductance measurement waveforms

drop across SiC MOSFET $v_{ds} = R_{ds(on)}(@v_{gs} = V_{GG})\ i_d$. Similarly drop across SiC SBD is $v_D = (V_{TD} + R_D i_d)$. R_d is the high frequency resistance of the power loop. Then the time evolution of $i_d(t)$ is given in (2) where $R_{on} = \left(R_{ds(on)} + R_D + R_d\right)$.

$$i_d(t) = \left(\frac{V_{dc} - V_{TD}}{R_{on}}\right)\left(1 - e^{-\frac{R_{on}t}{L_d + L_s}}\right) \tag{2}$$

$(L_d + L_s)$ and R_d calculated for C2M0080120D MOSFET and C4D10120A diode pair and $V_{dc} = 5V$, $V_{GG} = 20V$, $V_{CC} = -5V$. $R_{ds(on)} = 80m\Omega\ @v_{gs} = 20V$, $V_{TD} = 0.92V$ and $R_D = 56m\Omega$ is obtained from the datasheet. All measurements are done at 25^oC. $(L_d + L_s) \approx 70nH$ and $R_d \approx 47m\Omega$ is used and experiment and closed form expression matches closely.

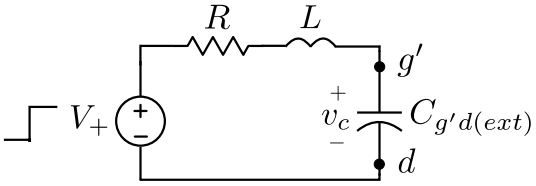

Fig. 5. Equivalent RLC circuit

v_{gs} during current rise period in SiC MOSFET and SBD pair during turn on transition can be represented explicitly

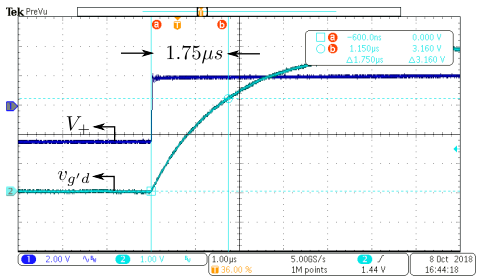

Fig. 6. Experimental waveform

as a function of time (3). For low R_{gext} and high value of I_0, $R_g C_{gs} \ll \beta L_s (V_{GG} - V_{th})$ and $\left(\frac{v_{gs} - V_{th}}{V_{GG} - V_{th}}\right) \ll 1$. Neglecting $R_g C_{gs}$ and approximating the logarithmic term upto second degree polynomial and using (1), we can represent the rate of change of i_d approximately using (4) [4]. So value of L_s can be computed using (4) and the value of (di_d/dt) is obtained experimentally.

$$\begin{aligned} t =& \varphi(v_{gs}) \\ =& -\left(R_g C_{gs} + \beta L_s (V_{GG} - V_{th})\right) \ln\left(1 - \frac{v_{gs} - V_{th}}{V_{GG} - V_{th}}\right) \\ & - \beta L_s (v_{gs} - V_{th}) \end{aligned} \tag{3}$$

$$\frac{di_d}{dt} \approx \frac{(V_{GG} - V_{th})}{L_s} \tag{4}$$

We have calculated the value of d for the operating condition $V_{dc} = 800V$, $i_d = 20A$ and $V_{GG} = 20V$ and $R_{gext} = 2.5\Omega$ from experiment and it coming out to be equal to $1.93A/ns$. So using the above expression $Ls = 7.5ns$. Then $L_d \approx (70 - 7.5) = 63.5nH$.

To verify the correctness of the model, Spice based simulation is performed with the previously obtained values (Fig. 4(a)) of L_d and L_s. A good agreement is observed between Spice based simulation and experimentally obtained waveforms (see Fig. 4(b)).

IV. $C_{g'd(ext)}$ AND $C_{ak(ext)}$ MEASUREMENT

$C_{g'd(ext)}$ and $C_{ak(ext)}$ both are constant capacitances and depend on the PCB layout and the dielectric material used (FR4 for our case). The value of this parasitic capacitances are in the order of picofarad range and difficult to measure using any common capacitance measuring instrument. The procedure for extracting $C_{g'd(ext)}$ is explained here. Same steps have been followed for $C_{ak(ext)}$.

Note that the MOSFET package does not contribute to this capacitance, as the terminal characteristics of the packaged device is given in the datasheet. As $C_{g'd(ext)}$ is due to the external circuit configuration, during this test the SiC MOSFET was disconnected. To measure $C_{g'd(ext)}$, a resistance, R (100 kΩ range) is connected in series with the capacitance (gate and

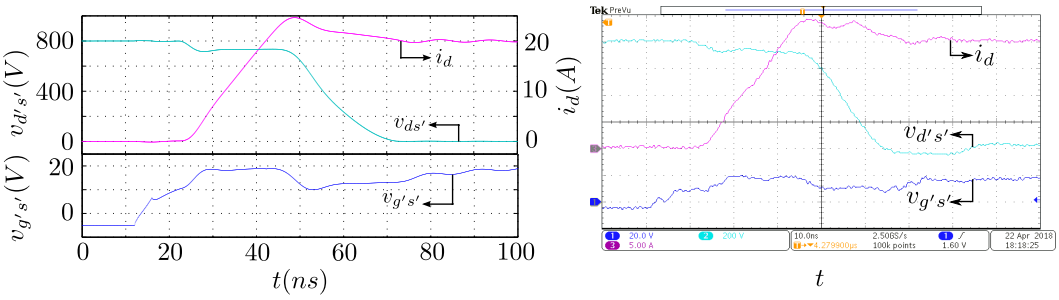

Fig. 7. Operating conditions: [800V, 8.5Ω, 20A] (a) Simulation waveforms, (b) Experimental waveforms: i_d (5A/div.), $v_{ds'}$ (200V/div.), $v_{g's'}$ (20V/div.) and t (10ns/div.)

drain pads are accessible in the PCB. Two small wires have soldered on these pads and a resistance is connected externally in series). There will always be some inductances (L) in the circuit because of resistance leads and connecting wires (in the range of nH). This will form a series RLC circuit (Fig. 5). Step voltage excitation from zero to V_+ level is given and the voltage across $C_{g'd(ext)}$ (v_c) is measured.

Applying KVL in Fig. 5, we get (5). For this circuit damping factor $\zeta = \left(\frac{R}{2}\right)\sqrt{\frac{L}{C_{g'd(ext)}}} \gg 1$ and $\left(\frac{4C_{g'd(ext)}}{R^2L}\right) = x \ll 1$, so the roots are real. Initial conditions are $v_c(0) = 0$, $\left.\frac{dv_c}{dt}\right|_{t=0} = 0$ and final condition is $v_c(\infty) = V_+$. Then $v_c(t)$ can be written in the form (6), where $A_1 = \frac{V_+}{\left(1 - \frac{p_1}{p_2}\right)}$, $A_2 = \frac{V_+}{\left(\frac{p_2}{p_1} - 1\right)}$. Then $p_1 \approx \frac{1}{RC_{g'd(ext)}}$ and $p_2 \approx \frac{R}{L}$ as $x \ll 1$. As the value of R is large such that $p_1 \ll p_2$. Then $A_1 \approx -V_+$ and $A_2 \approx 0$. So the effect of $A_2e^{-p_2t}$ can be neglected and $v_c(t) \approx V_+\left(1 - e^{-p_1t}\right)$. So approximately it becomes a RC series circuit.

$$v_c(s) = \frac{V_+}{s}\left(\frac{1}{LC_{g'd(ext)}s^2 + RC_{g'd(ext)}s + 1}\right) \quad (5)$$

$$v_c(t) = V_+ + A_1e^{-p_1t} + A_2e^{-p_2t} \quad (6)$$

$V_+ = 5V$, $R = 100k\Omega$ and $\tau = RC_{g'd(ext)} = 1.75\mu s$ is the time required for $v_c(t)$ to change from zero to $0.63V_+$ (Fig. 8). $C_{g'd(ext)} = \tau/R = 17.5pF$. Passive probe TPP1000 from Tektronix is used for voltage measurement which has a input capacitance of $< 4pF$ (given in the datasheet of TPP1000). This capacitance will come in parallel with $C_{g'd(ext)}$. We have assumed it's value is around $4pF$. Then $C_{g'd(ext)} \approx 13pF$. Similarly $C_{ak(ext)} \approx 14pF$ is obtained.

V. Validation of the Proposed Method through Turn on Switching Transient

To validate the correctness of the experimentally determined external circuit parasitics, switching transient model described in Fig. 1 is simulated for turn on switching transient (with the estimated values of the external circuit parasitics) and compared with the experimentally obtained turn on switching transient. Fig. 7 shows such a case where $V_{dc} = 800V$, $I_0 = 20A$ and $R_{gext} = 8.5\Omega$. A close agreement between simulation and experiment is observed. This validates the correctness of the experimentally obtained external circuit parasitics. The effect of different circuit parasitics is be given in [3].

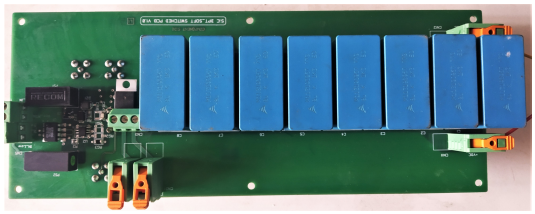

Fig. 8. Experimental setup

VI. Conclusion

A simple experimental measurement based approach to determine the external circuit parasitics relevant for switching transient study of SiC MOSFET and SBD diode pair has been proposed in this literature. The estimated parasitic values are verified using double pulse test. A close agreement between simulated and experimentally obtained turn on transient is observed.

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